DESIGN OF A CCII-BASED PIPELINE A/D CONVERTER

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ABSTRACT

Nowadays electronic applications, including wireless communication, imaging and video, demand high-resolution and low-distortion analog-to-digital conversion (ADC) with a signal bandwidth of tens of MHz. This paper reports a design of a pipeline ADC using second-generation current conveyor (CCII) and this used CCII is based on CMOS inverter. Simulation is done in cadence environment with 0.18 µm technology using Virtuoso simulator. Simulation results are reported that shows the capability and effectiveness of the proposed design. Authors have verified the capability of this design to operate over the high frequency range (10 to 100MHz). Best simulation results obtained on cadence environment with 180nm technology. Also the layout design is carried out and verified the performance of the proposed 10 bit ADC design. Finally a result of complete ADC design is reported and compared with earlier reported work. This design will be beneficial for young designers and manufacturers.

KEYWORDS: Pipelined ADC, Current Conveyor, Cadence, CMOS Inverter and Resolution